	US ATLAS **HL-LHC Upgrade** **BASIS of ESTIMATE (BoE)**	**Date of Est:** **22-Nov-2015** **Prepared by:** **Joey Huston (Michigan State University)** **Docdb #:**

WBS number: 6.5.3.4	**WBS Title: Tile Calorimeter DCS and ELMB++ Motherboards**

WBS Dictionary Definition:

This WBS covers the design and fabrication of the motherboard for the new ELMB++ board to be designed for the Tilecal HL-LHC running. The ELMB++ (and its motherboard) is an integral part of DCS control for the Tilecal. The plan is for the new ELMB++ board to allow for greater diagnostic capability for Low Voltage Power Supply failures. The new motherboard, which is mounted in the LV finger box, has to be capable of supporting those new features.

The deliverables for WBS 6.5.3.4 are: (1) design of a new motherboard, (2) prototyping of that board, (3) design and production of test equipment for the motherboard, (4) production of 256 ELMB++ motherboards boards over a two-year period, and (5) follow-up of the integration of the ELMB++ motherboards in the Tilecal LVPS system. Items 1 and 2 are not part of project costs, but will be covered by prototyping/R&D funding. Additional tasks are parts procurement and monitoring of outsourced assembly, elevated temperature burn-in of cards with testing and repair.

Estimate Type (check all that apply – see BOE Report for estimate type by activity):

___ Work Complete
___ Existing Purchase Order
___ Catalog Listing or Industrial Construction Database
___ Documented Vendor Estimate based on Drawings/ Sketches/ Specifications
_x__ Engineering Estimate based on Similar Items or Procedures
___ Engineering Estimate based on Analysis
_x__ Expert Opinion

Supporting Documents (including but not limited to):

Attachments:

Details of the Base Estimate (explanation of the Work)

This BOE covers the production of 100% of the ELMB++ mother-boards needed for the detector. The effort includes purchasing components and PCBs for the 256 units needed, and shipping of the boards to CERN.

The ELMB++ Motherboard is an 8-layer PCB that interfaces between the LV power brick controller and the CERN-produced ELMB++ DCS communication board. Based on past experience, we will find a vendor for production and assembly of the motherboard. Components will be chosen by MSU with input from the vendor. The plan is for the assembly process to be monitored at the beginning of production, by an experienced electrical engineer (EE) from MSU present at the assembly house. Further quality checks will be made after the assembled boards arrive back from the assembly house, by the EE and ET, in order to detect and repair faults.

The assembled boards will be received from the vendor at Michigan State University where they will be mounted in burn-in fixtures and monitored in real times at elevated temperatures. Any problem diagnosis and repair will be performed both by the EE and the ET. Undergraduate students will be employed to mount the boards in the burn-in fixtures, monitor them periodically, and to dismount and store units that pass the criteria. Shipping the tested boards to CERN will incur materials and ET labor costs. It will be necessary for the EE to spend significant time at CERN to acceptance test the boards after they are received and mounted in the fLVPS boxes.

Cost of components and PCBs has been estimated from experience with the previous version of the ELMB++ mother-boards and recent experience with similar boards.

Labor FTEs are based on experience with the previous version of the ELMB++ mother-boards and with similar projects. The breakdown is as follows:

1. Final design: 34% FTE EE in FY19.
2. Vendor selection, component selection and BoM: 6% FTE EE in FY20
3. Component/PCB testing for prototyping: 2.8% FTE ET in FY20
4. Oversee PCB assembly, initial testing, debugging with assy hse for prototyping: 23% FTE EE, 23% FTE ET in FY20
5. Test equipment fabrication: 14% FTE EE, 9% FTE ET in FY20
6. Oversee PCB assembly, testing, full production: 6% FTE EE in FY21 and 6% FTE EE in FY22
7. Mount in burn-in fixtures; supervise students, full production: 3% ET, 0.3 FTE UG in FY21 and FY22
8. Diagnose and repair failures, full production: 6% EE and 3% ET in FY21 and FY22
9. Inventory, crate and ship to CERN, full production: 1% ET in FY21 and FY22
10. Acceptance testing at CERN and system integration: 23% EE in FY23

Costs under categories 1-4 are considered to be covered by the prototyping/R&D phase budget. Costs 5-10 are considered to be project costs.

Travel to CERN by the EE is needed during the production phase to attend expert weeks and to conduct the acceptance tests. We have estimated that three week-long trips per year will be necessary in 2019-22. Two five-week trips to CERN by the EE are planned for the integration phase in 2023.

A cost summary for the production phase is tabulated below.

WBS	Deliverable	Task	Labor Hrs	Labor $	M&S $	Travel $	Total $
6.5.3.4	**ELMB++ Motherboards**		**3,470**	**213,621**	**120,440**	**45,000**	**379,061**
	Parts Procurement/Q&A	DCS3020	150	11,746	14,080	1,000	26,826
	Engineering labor		150				
	Student labor		0				
	Burn-in/Test/repair	DCS3030	800	59,042	0	9,000	68,042
	Engineering labor		800				
	Student labor		0				
	Test Equipment fabrication	DCS3040	400	30,602	40,000	0	70,602
	Engineering labor		400				
	Student labor		0				
	Parts Procurement/Q&A	DCS3120	200	18,255	63,360	2,000	83,615
	Engineering labor		200				
	Student labor		0				
	Burn-in/Test/repair	DCS3130	1,800	86,298	0	33,000	119,298
	Engineering labor		800				
	Student labor		1,000				
	Shipping	DCS3210	120	7,678	3,000	0	10,678
	Engineering labor		120				
	Student labor		0				

Schedule:

ATLAS management has scheduled installation of the Tile Calorimeter modules to begin early in 2024; possibly even late 2023. Consequently, the complete number of 256 tested and assembled LVPS units must be ready by 2023Q4. These requirements call for the following timeline:

1. 2018-19: final design and prototype pre-production
2. 2020: parts procurement, production and testing of 30 prototype boards
3. 2021: parts procurement, production and testing of 128 boards
4. 2022: parts procurement, production and testing of 128 boards
5. 2023: acceptance testing at CERN and mounting on drawer structures

Costs under items 1 and 2 are considered to be covered by the prototyping/R&D phase. Costs under items 3-5 are considered to be covered by the project phase.

Assumptions:

- New ELMB board will be supplied by CERN; the Tilecal group will provide input to CERN to insure the relevant functionality is present on the new ELMB board.

Risk Analysis

Schedule Risk:

Probability: Low

Potential Problem: Delay in receiving new ELMB boards from CERN.

Mitigation: Design effort can continue if details of new ELMB boards are available.

Cost Risk:

Probability: Low

The motherboard consists of standard, low-tech components.

Technical/Scope Risk:

Probability: Low

The ELMB++ is designed to be the standard for all DCS communications, and Tilecal experts are participating in the design.

M&S Contingency Rules Applied

50%

We now estimate the contingency based on the rules for M&S. It depends on the maturity of the cost estimate.

5) 40-60% contingency on: items with a detailed conceptual level of design; items adapted from existing designs but with extensive modifications, and/or made more than 2 years previous with documented costs. A physicist or engineering estimate uses this level.

Labor Contingency Rules Applied

50%

We now estimate the contingency based on the rules for Labor.. It depends on the maturity of the cost estimate.

> 40-60% contingency for a task that is not yet completely defined, but is analogous to past activities; for example, a fabrication activity similar to, but not exactly like, items fabricated for other activities; for example, design labor for items similar to, but not exactly like, previous designs.

Comments:

Attachments: